UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/511,512	10/14/2004	Jeroen Anton Johan Leijten	NL02 0321 US	4657

65913 7590 07/28/2008

NXP, B.V.
NXP INTELLECTUAL PROPERTY DEPARTMENT
M/S41-SJ
1109 MCKAY DRIVE
SAN JOSE, CA 95131

EXAMINER	
GIROUX, GEORGE	

ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
07/28/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/511,512	LEIJTEN, JEROEN ANTON JOHAN	
	Examiner	Art Unit	
	George D. Giroux	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 April 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed 21 April 2008, in response to the Office Action mailed 22 October 2007. The applicant's remarks and amendments to the claims and specification were considered, with the results that follow.

2. Claims 1-7 remain pending in this application.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slavenburg (US 6,122,722) in view of Martonosi (US 6,745,336).

As per claim 1, Slavenburg teaches a multi-issue processor comprising a register file as **[the register file 403 of a VLIW processor with multiple issue slots, ISSUE 1-3 (figure 3)],** a plurality of issue slots each comprising a plurality of functional units as **[issue slots 1-3 (figure 3) where the processor has less issue slots than there are functional units in the machine. As an example, for a machine with 7 functional units, 3 issue slots may suffice. In general, the number of issue slots for a given number and type of functional units is a tradeoff between average performance**

and cost (column 3, lines 49-56)], an input routing network as **[switching matrix 401 (figure 3)]** that provides multiple data path outputs for a single data path input, the input routing network receiving data from the register file on the single data path input via a single data input path and providing data from the register file to functional units of the plurality of functional units, the data provided on the multiple data path outputs via multiple data output paths as **[switching matrix 401, controlled by the input switch control 902, determines which read port (input path) to connect to the inputs of which functional unit (output paths) (column 4, lines 1-3 and figure 3)]**.

Slavenburg does not teach a plurality of holdable registers that hold duplicate data from the register file, and wherein in a first set of the plurality of issue slots the holdable registers store data on the multiple data output paths of the first set and in a second set of the plurality of issue slots the holdable registers store data on the single data input path corresponding to the input routing networks of the second set.

Martonosi teaches a plurality of holdable registers that hold duplicate data from the register file as **[input latches A (30 and 32) and B (34 and 36) (figure 1)]**, wherein in a first set of the plurality of issue slots the holdable registers store data on the multiple data output paths of the first set and in a second set of the plurality of issue slots the holdable registers store data on the single data input path corresponding to the input routing networks of the second set as **[input latches 30, 32, 34 and 36, for input operands A and B sit at the inputs to the functional unit 40 holding the operands from the registers (received via lines 60 and 62) (column 4, lines 30-38 and figure 1)]** wherein the switching matrix taught by Slavenburg (described above) sits at the

inputs of the functional units, and putting the holdable registers before or after the switching matrix is purely a matter of design choice.

Slavenburg and Martonosi are analogous art, as they are within the same field of endeavor, namely instruction processing.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine the VLIW processor with a switching matrix controlling the inputs of the functional units, taught by Slavenburg, with the input latches taught by Martonosi.

The motivation for doing so, as provided by Martonosi, would have been **[to reduce the power used in the microprocessor by detecting and disabling a predetermined number of bits that are not required for execution in the functional unit, using the operands within the input latches (column 4, lines 39-54)]**.

As per claim 3, Slavenburg teaches wherein the input routing network of each of the plurality of issue slots has a plurality of data path inputs as **[switching matrix 401, controlled by the input switch control 902, determines which read port (input paths) (such as R_{1a}-R_{3b}) to connect to the inputs of which functional unit (output paths) (column 4, lines 1-3 and figure 3)]**.

Slavenburg does not teach in the second set of issues lots holdable registers of the plurality of holdable registers are located between each of the inputs of the input routing network and the register file, however.

Martonosi teaches in the second set of issues lots holdable registers of the plurality of holdable registers are located between each of the inputs of the input routing network and the register file as **[input latches 30, 32, 34 and 36, for input operands A and B sit at the inputs to the functional unit 40 holding the operands from the registers (received via lines 60 and 62) (column 4, lines 30-38 and figure 1)]** wherein the switching matrix taught by Slavenburg (described above) sits at the inputs of the functional units, and putting the holdable registers before or after the switching matrix is purely a matter of design choice.

Slavenburg and Martonosi are analogous art, as they are within the same field of endeavor, namely instruction processing.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to combine the VLIW processor with a switching matrix controlling the inputs of the functional units, taught by Slavenburg, with the input latches taught by Martonosi.

The motivation for doing so, as provided by Martonosi, would have been **[to reduce the power used in the microprocessor by detecting and disabling a predetermined number of bits that are not required for execution in the functional unit, using the operands within the input latches (column 4, lines 39-54)]**.

As per claim 4, Martonosi teaches wherein, in the first set of issue slots, holdable registers are located between the input routing networks and each of the plurality of function units as **[input latches 30, 32, 34 and 36, for input operands A and B sit at**

the inputs to the functional unit 40 holding the operands from the registers (received via lines 60 and 62) (column 4, lines 30-38 and figure 1)].

5. Claims 2 and 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Slavenburg (US 6,122,722) in view of Martonosi (US 6,745,336), as applied to claim 1 above, and further in view of Fisher (US 6,026,479).

As per claim 2, Slavenburg teaches the multi-issue processor of claim 1, in view of Martonosi, as described above.

Slavenburg does not teach "a first instruction set accessing at least the first set of issue slots; and a second instruction set accessing the second set of issue slots", however.

Fisher teaches "a first instruction set accessing at least the first set of issue slots; and a second instruction set accessing the second set of issue slots" as **["A CPU having a cluster VLIW architecture...which operates in both a high instruction level parallelism (ILP) mode and a low ILP mode. In high ILP mode, the CPU executes wide instruction words using all operational clusters of the CPU and all of a main instruction cache and main data cache of the CPU are accessible to a high ILP task. The CPU also includes a mini-instruction cache, a mini-instruction register and a mini-data cache which are inactive during high ILP mode. An instruction level controller in the CPU receives a low ILP signal, such as an interrupt or function call to a low ILP routine, and switches to low ILP mode. In low ILP mode, the main instruction cache and main data cache are deactivated to**

preserve their contents. At the same time, a predetermined cluster remains active while the remaining clusters are also deactivated. The low ILP task executes instructions from the mini-instruction cache which are input to the predetermined cluster through the mini-instruction register. The mini-data cache stores operands for the low ILP task"(abstract, lines 1-19)].

Slavenburg and Fisher are analogous art, as they are within the same field of endeavor, namely VLIW processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the VLIW processor with a switching matrix controlling the inputs of the functional units, taught by Slavenburg, with the multiple instruction sets of Fisher.

The motivation for doing so is provided by Fisher as **["the separate mini-instruction cache and mini-data cache along with the use of only the predetermined cluster minimizes the pollution of the main instruction and data caches, as well as pollution of register files in the deactivated clusters, with regard to a task executing in high ILP mode"(abstract, lines 20-24)]**.

As per claim 5, Slavenburg teaches the multi-issue processor of claim 1, in view of Martonosi, as described above.

Slavenburg does not teach wherein the first set of issue slots are accessed by a first set of instructions for a VLIW processor and the second set of issue slots are accessed by a second set of instructions that are used by an interrupt routine, however.

Fisher teaches wherein the first set of issue slots are accessed by a first set of instructions for a VLIW processor and the second set of issue slots are accessed by a second set of instructions that are used by an interrupt routine as **["A CPU having a cluster VLIW architecture…which operates in both a high instruction level parallelism (ILP) mode and a low ILP mode. In high ILP mode, the CPU executes wide instruction words using all operational clusters of the CPU and all of a main instruction cache and main data cache of the CPU are accessible to a high ILP task. The CPU also includes a mini-instruction cache, a mini-instruction register and a mini-data cache which are inactive during high ILP mode. An instruction level controller in the CPU receives a low ILP signal, such as an interrupt or function call to a low ILP routine, and switches to low ILP mode. In low ILP mode, the main instruction cache and main data cache are deactivated to preserve their contents. At the same time, a predetermined cluster remains active while the remaining clusters are also deactivated. The low ILP task executes instructions from the mini-instruction cache which are input to the predetermined cluster through the mini-instruction register. The mini-data cache stores operands for the low ILP task"(abstract, lines 1-19)]**.

Slavenburg and Fisher are analogous art, as they are within the same field of endeavor, namely VLIW processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the VLIW processor with a switching matrix controlling the

inputs of the functional units, taught by Slavenburg, with the multiple instruction sets of Fisher.

The motivation for doing so is provided by Fisher as **["the separate mini-instruction cache and mini-data cache along with the use of only the predetermined cluster minimizes the pollution of the main instruction and data caches, as well as pollution of register files in the deactivated clusters, with regard to a task executing in high ILP mode"(abstract, lines 20-24)]**.

As per claim 6, Fisher teaches wherein the second set of instructions has fewer instructions than the first set of instructions as **[An embodiment of a method for reducing cache pollution in a CPU, according to the present invention, includes providing a main instruction cache configured to store VLIW instructions, wherein each VLIW instruction is further comprised of a plurality of c-instructions, providing a plurality of operational clusters, wherein each one of the plurality of operational clusters is configured to receive one of the plurality of c-instructions of each VLIW instruction in the main instruction cache, and executing a high ILP task by loading VLIW instructions from the main instruction cache into a main instruction register for output to the plurality of clusters. The method includes receiving a low ILP signal and, responsive thereto, deactivating the main instruction cache and main instruction register, deactivating the plurality of operational clusters, except for a predetermined one of the operational clusters, activating a mini-instruction cache and a mini-instruction**

register, and serially executing a low ILP task by serially loading c-instructions from the mini-instruction cache into the mini-instruction cache for output to the predetermined one of the operational clusters (column 4, lines 16-34)].

As per claim 7, Slavenburg teaches the multi-issue processor of claim 1, in view of Martonosi, as described above.

Slavenburg does not teach wherein the first set of issue slots has more issue slots than the second set of issue slots, however.

Fisher teaches wherein the first set of issue slots has more issue slots than the second set of issue slots as **["The CPU also includes a mini-instruction cache, a mini-instruction register and a mini-data cache which are inactive during high ILP mode. An instruction level controller in the CPU receives a low ILP signal, such as an interrupt or function call to a low ILP routine, and switches to low ILP mode. In low ILP mode, the main instruction cache and main data cache are deactivated to preserve their contents. At the same time, a predetermined cluster remains active while the remaining clusters are also deactivated. The low ILP task executes instructions from the mini-instruction cache which are input to the predetermined cluster through the mini-instruction register. The mini-data cache stores operands for the low ILP task"(abstract, lines 6-19) wherein deactivating some clusters means the cluster running the low ILP tasks (the second set of issue slots) is smaller than the first]**.

Slavenburg and Fisher are analogous art, as they are within the same field of endeavor, namely VLIW processing.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to combine the VLIW processor with a switching matrix controlling the inputs of the functional units, taught by Slavenburg, with the multiple instruction sets of Fisher.

The motivation for doing so is provided by Fisher as **["the separate mini-instruction cache and mini-data cache along with the use of only the predetermined cluster minimizes the pollution of the main instruction and data caches, as well as pollution of register files in the deactivated clusters, with regard to a task executing in high ILP mode"(abstract, lines 20-24)]**.

Response to Arguments

6. Applicant's arguments filed 21 April 2008 have been fully considered but they are not persuasive.

7. In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

8. In either case, that the latches (i.e., holdable registers) taught by Martonosi are placed before the switching matrix, taught by Slavenburg, or after, the latches operate the same, and will still hold the operand inputs being sent to the functional units. Therefore the placement of the latches/registers before or after the switching matrix, when the matrix is merely directing the inputs to the correct unit, is purely a matter of design choice. The fact that applicant has recognized another advantage to the placement which would flow naturally from following the suggestion of the prior art cannot be the basis for patentability when the differences would otherwise be obvious. See *Ex parte Obiaya*, 227 USPQ 58, 60 (Bd. Pat. App. & Inter. 1985).

Conclusion

9. The following is a summary of the treatment and status of all claims in the application as recommended by **M.P.E.P. 707.07(i)**: claims 1-7 are rejected.

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. The examiner requests, in response to this Office action, support be shown for language added to any original claims on amendment and any new claims. That is, indicate support for newly added claim language by specifically pointing to page(s) and line number(s) in the specification and/or drawing figure(s). This will assist the examiner in prosecuting the application.

12. When responding to this office action, Applicant is advised to clearly point out the patentable novelty which he or she thinks the claims present, in view of the state of the art disclosed by the references cited or the objections made. He or she must also show how the amendments avoid such references or objections. See 37 CFR 1.111(c).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to George D. Giroux whose telephone number is (571)272-9769. The examiner can normally be reached on Monday through Friday, 9:30am - 6:00pm E.S.T.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie P. Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Eddie P Chan/
Supervisory Patent Examiner, Art Unit 2183

/George D Giroux/
Examiner, Art Unit 2183